Scheduling Multi-Mode Real-Time Systems upon Uniform Multiprocessor Platforms

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Abstract

In this paper, we address the scheduling problem of multi-mode real-time systems upon uniform multiprocessor platforms. We propose two transition protocols, specified together with their schedulability test, and provide the reader with two distinct upper bounds for the length of the transient phases during mode transitions, respectively for the cases where jobs priorities are known and unknown beforehand.

1. Introduction

Over the years, the sporadic constrained-deadline task model \cite{4} has proven remarkably useful for the modeling of recurring processes that occur in hard real-time computer application systems, where the failure to satisfy any constraint may have disastrous consequences. The problem of scheduling a single set of such tasks so that all the deadlines are met has been widely studied in the literature. However, many applications exhibit multiple behaviors issued from several operating modes (e.g., an initialization mode, an emergency mode, a fault recovery mode, etc.), where each mode is characterized by its own set of tasks. During the execution of such multi-mode hard real-time systems, switching from the current mode (called old-mode) to another mode (called new-mode) requires to substitute the current executing task set with the one of the new-mode. This substitution introduces a transient phase, where the tasks of the old-mode may be scheduled together with those of the new-mode, which could lead to an overload that can jeopardize the system schedulability. In a multi-mode real-time system, any Mode Change Request (MCR) divides the timeline into the alternance of two phases: (i) A steady phase before the MCR occurs, and (ii) a transient phase during the mode change.

In the presence of a MCR, a task $\tau_i$ can be classified according to its behavior during the transition. Thus, we distinguish between old-mode and new-mode tasks, see \cite{10} for details. If $\tau_i$ belongs to the old-mode, then it may require to complete the execution of its current active job or it could be aborted at the occurrence of the MCR. The abortion is performed when it is feasible without loss of data consistency. In this paper, we will assume that every old-mode job must complete its execution when a MCR occurs which is actually the worst-case. If $\tau_i$ belongs to the new-mode, then it could either be a completely new task, that is, it does not belong to the old-mode but is active in the new one, or it could be active in both modes, such that its sporadic execution pattern must not be jeopardized by the occurrence of the MCR. In this latter case, it is said to be mode-independent. Due to the difficulty to guarantee the schedulability of such tasks, we only consider systems without mode-independent tasks in this research.

If a transition protocol allows the management of mode-independent tasks, then it is said to be with periodicity, otherwise it is said to be without periodicity. Moreover if it allows to schedule new-mode tasks only when all old-mode ones are completed, then it is said to be synchronous, otherwise it is said to be asynchronous.

Related work. Up to now, the scheduling of multi-mode hard real-time systems has been much studied, particularly upon uniprocessor platforms, where there is only one shared processor available upon which all the jobs must be executed \cite{1, 11}. Recently, extensive efforts have been performed towards extending the uniprocessor results to multiprocessor platforms, where there are several shared processors available upon which jobs may execute. Sound results have been obtained in the particular case of identical multiprocessor platforms \cite{8, 9}.

This research. In this paper, we study the scheduling of multi-mode hard real-time systems upon uniform multiprocessor platforms. We propose two protocols – a synchronous and an asynchronous one – for managing the mode transitions. Note that the results presented here...
also hold for identical multiprocessor platforms as they are a special case of uniform multiprocessor platforms, in which the computing capacities of all processors are equal.

**Paper organization**. The remainder of this paper is structured as follows. Section 2 presents the platform and system model, as well as the scheduler and the mode transition specifications that are used throughout the paper. Section 3 provides the reader with some useful definitions and observations. Section 4 introduces two protocols – a synchronous and an asynchronous one – for managing the mode transitions during the execution of a multi-mode hard real-time systems upon a uniform multiprocessor platform. Section 5 provides sufficient conditions under which a given system can be executed on a given platform without missing any deadline. Section 6 elaborates these conditions for the specific cases where jobs priorities are known and unknown beforehand. Section 7 presents experimental results. Finally, Section 8 concludes the paper and proposes future work.

2. Model of computation

2.1. Multi-mode real-time specifications

We consider a multi-mode real-time system to be a set of $x$ operating modes $M^1, M^2, \ldots, M^x$ such that the operating mode $M^k$ has to execute the task set $\tau^k \equiv \{\tau^k_1, \tau^k_2, \ldots, \tau^k_n\}$ consisting of $n_k$ tasks by following the scheduler $S^k$. Each task $\tau^k_i$ is modeled by a sporadic constrained-deadline task characterized by three parameters $(C^k_i, D^k_i, T^k_i)$ where $C^k_i$ is the Worst Case Execution Time (WCET), $D^k_i \leq T^k_i$ is the relative deadline and $T^k_i$ is the minimum inter-arrival time between two consecutive releases of $\tau^k_i$. These parameters are given with the interpretation that, during the execution of mode $M^k$, task $\tau^k_i$ generates a certain number of successive jobs $\tau^k_{ij}$ with execution requirement of at most $C^k_i$ each, arriving at time $a^k_{ij}$ such that $a^k_{ij} \geq D^k_i$ and that must complete within $[a^k_{ij}, a^k_{ij} + D^k_i]$ where $a^k_{ij} \equiv a^k_{ij} + D^k_i$. Job $\tau^k_{ij}$ is said to be active if and only if $a^k_{ij} \leq t$ and is not completed yet. More precisely, an active task is said to be running at time $t$ if it is allocated to a processor and is being executed. Otherwise the active task is in the ready queue of the operating system and it is said to be ready. We denote by $active(\tau^k, t)$, $run(\tau^k, t)$ and $ready(\tau^k, t)$ the subsets of active, running and ready tasks of $\tau^k$ at time $t$, respectively. It holds that $active(\tau^k, t) \equiv run(\tau^k, t) \cup ready(\tau^k, t)$. Except during the transition phases, we assume that the system always runs in only one mode and that all the tasks are independent, i.e., there is no communication, no precedence constraint and no shared resource (except for the processors) between tasks.

At run-time, every task in the system must be enabled before it can generate jobs, otherwise it is disabled. When all the tasks in $\tau^k$ are enabled and all the tasks in other modes are disabled, the system is said to be running in mode $M^k$. As such disabling $\tau^k_j$ prevents future job arrivals from $\tau^k_j$. We denote the subsets of enabled and disabled tasks of $\tau^k$ at time $t$ by enabled($\tau^k, t$) and disabled($\tau^k, t$), respectively.

We denote a Mode Change Request (MCR) from a given mode, say $M^i$, to a new mode, say $M^j$, by $I_{M^i\rightarrow M^j}$ and we denote the invocation time of a MCR by $t_{M^i\rightarrow M^j}$. At the occurrence of a MCR the active old-mode jobs are called rem-jobs and must complete their execution as it has been assumed in Section 1. Note that the results that we are presenting in this paper also hold when some rem-jobs can be aborted at $t_{M^i\rightarrow M^j}$ since such jobs do not jeopardize the system schedulability.

Because the rem-jobs may cause an overload if the tasks of $\tau^k$ are immediately enabled upon a MCR($\tau^k$), the transition protocols sometimes have to delay the time at which they enable the new-mode tasks until it is safe to do so. Consequently, we denote by $D^k_{M^i\rightarrow M^j}$ the relative mode-change deadline of task $\tau^k_j$ during the transition from mode $M^i$ to mode $M^j$, with the interpretation that the transition protocol must ensure that $\tau^k_j$ is not enabled after time $t_{M^i\rightarrow M^j} + D^k_{M^i\rightarrow M^j}$. The system enters mode $M^j$ as soon as all the rem-jobs are completed and all the tasks of $\tau^j$ are enabled.

2.2. Platform specifications

We consider the scheduling of multi-mode hard real-time systems upon a uniform multiprocessor platform comprised of $m$ processors. We denote the $m$-processor uniform platform by $\pi = [s_1, s_2, \ldots, s_m]$ where each processor $\pi_i$, $i = 1, 2, \ldots, m$ is characterized by its own speed or computing capacity $s_i$, with the interpretation that a job that executes on a processor $\pi_i$ for $t$ time units completes $(s_i \cdot t)$ units of execution. For reasons of clarity and readability, we assume without any loss of generality that $s_i \leq s_{i+1}$ for $i = 1, 2, \ldots, m-1$ and $s_1 > 0$.

2.3. Scheduler specifications

We consider that every mode $M^k$ uses its own scheduler denoted by $S^k$ which can be either Fixed-Task-Priority (FTP) or Fixed-Job-Priority (FJP). FTP schedulers assign a priority to each task at system design-time (i.e., before the system execution) and then, at run-time, every released job inherits the priority of the task it belongs to. Conversely, FJP schedulers determine the priority of each job at run-time and different jobs of the same task may have different priorities. However, for both FTP and FJP schedulers, the priority of each job may not change between its release time and its completion time. Additionally, these two types of schedulers are assumed to be work-conserving according to the following definition.

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3 According to these interpretations, the FTP schedulers are a particular case of the FJP schedulers, in which the priorities of all jobs issued from the same task are all equal to the same value determined beforehand.
Definition 1 (Work-conserving schedulers) A scheduler is said to be work-conserving upon an m-processor uniform platform if and only if it satisfies the following conditions:

- A processor cannot be idle if there are active ready jobs.
- If at some time instant there are fewer than m active ready jobs (recall that m denotes the number of processors in the uniform multiprocessor platform), then the active ready jobs are executed upon the fastest processors. That is, at any time instant t if the j’th-slowest processor is idled by the scheduler, then the k’th-slowest processor (∀k < j) is also idled at t.
- Higher priority jobs are executed upon faster processors.

Lemma 1 Let J be any set of synchronous jobs and π be any uniform platform. Let S denote the schedule of J produced on π by any work-conserving FJP scheduler. If step$_j$ denotes the smallest instant in S where at least j processors are idle, then it holds ∀j = 2,...,m that

$$\text{step}_j \geq \text{step}_{j-1}$$

Proof According to Definition 1, when a job completes on (or migrates from) any processor π$_j$ with j ∈ [2,m], the job (if any) executing on processor π$_{j-1}$ migrates to processor π$_j$. This directly leads to step$_j$ ≥ step$_{j-1}$ (see Figure 1).

2.4. Mode transition specifications

During the execution of a multi-mode real-time system in a given mode, say $M'$, we consider that a Mode Change Request MCR($j$) to the new mode $M'$ can be initiated by any task of $\tau'$ or by the system itself, whenever it detects a change in the environment or in its internal state. At that time the system entrusts the scheduling decisions to the transition protocol. Such a protocol immediately disables all the old-mode tasks, which thus prevents the system of new jobs arrival from these tasks. The goal of the transition protocol is to complete all the rem-jobs and to enable all the new-mode tasks while meeting all the job and mode-change deadlines. Once again we recall that we do not consider multi-mode real-time systems with mode-independent tasks. This study will be performed under the following assumptions during mode transitions: (i) Job migration is permitted (with no penalty). That is, a job that has been preempted on a particular processor may resume execution on the same or a different processor; (ii) Job parallelism is forbidden. That is, a job may execute on at most one processor at any given instant in time.

3. Definitions and observations

Before going any further in this paper, let us provide the reader with some useful definitions and observations.

Definition 2 (A valid protocol) A transition protocol is said to be valid for a given multi-mode real-time system if it always meets all the job and mode-change deadlines during the transition from any mode of the system to any other one.

Definition 3 ($S_\pi$) Let $\pi = [s_1,s_2,...,s_m]$ denote an m-processor uniform platform. We define $S_\pi$ as the sum of all the processor speeds, i.e., $S_\pi \overset{\text{def}}{=} \sum_{i=1}^{m} s_i$.

Definition 4 (Predictability) Let A denote a scheduler, and let $J = \{J_1,J_2,J_3,\ldots\}$ be a potentially infinite set of jobs, where each job $J_i = (a_i,c_i,d_i)$ is characterized by an arrival time $a_i$, a computation requirement $c_i$ and an absolute deadline $d_i$. Let $g_i$ (resp. $f_i$) denote the time at which job $J_i$ starts (resp. completes) its execution when $J$ is scheduled by A. Now consider any set $J' = \{J'_1,J'_2,J'_3,\ldots\}$ of jobs obtained from $J$ as follows. Job $J'_i$ is characterized by the arrival time $a_i$, a computation requirement $c_i' \leq c_i$ and the absolute deadline $d_i$. Let $g'_i$ (resp. $f'_i$) denote the time at which job $J'_i$ starts (resp. completes) its execution when $J'$ is scheduled by A. Algorithm A is said to be predictable if, and only if, for any set of jobs $J$ and any such $J'$ obtained from $J$, it is the case that $g'_i \leq g_i$ and $f'_i \leq f_i$ ∀i.

Lemma 2 (See [5]) Any work-conserving and FJP algorithm is predictable on uniform multiprocessor platforms.

Lemma 3 When a MCR($j$) occurs at time $t_{\text{MCR}(j)}$ while the system is running in mode $M'$, every rem-job issued from the tasks of $\tau'$ meets its deadline when scheduled by $S'$ upon an $m$-processor uniform platform.
Proof From our assumptions, we know that the set of tasks \( t' \) of the mode \( M' \) is schedulable by \( S' \) upon an \( m \)-processor uniform platform, and from Lemma 2 we know that \( S' \) is predictable. When the MCR\( (j) \) occurs at time \( t_{\text{MCR}}(j) \), all the tasks of \( t' \) are disabled. Disabling these tasks is equivalent to set the execution time of all their future jobs to zero, and since \( S' \) is predictable the deadline of every rem-job is still met.

Lemma 4 At the occurrence of a MCR\( (j) \) for the transition to an operating mode, say from mode \( M' \) to mode \( M^j \), the worst-case scenario (in terms of job completion time) is the one where all the rem-jobs issued from the tasks of \( t' \) are released simultaneously upon MCR\( (j) \) with a computation requirement equal to their WCET each.

Proof The property is straightforward from Lemma 2 and the fact that we only consider work-conserving schedulers in each operating mode. These ones are predictable.

Definition 5 (Makespan) Let \( J = \{J_1, J_2, \ldots, J_n\} \) be a set of \( n \) jobs, all released at time \( t = 0 \), with computation requirements \( C_1, C_2, \ldots, C_n \), respectively. Let \( \pi = [s_1, s_2, \ldots, s_m] \) denote an \( m \)-processor uniform platform and \( A \) be any scheduling algorithm. If \( S \) denotes the schedule of \( J \) produced by \( A \) upon \( \pi \) then \( \pi \) is the earliest instant in \( S \) at which all jobs of \( J \) are completed.

Very often, and especially when job priorities are unknown beforehand, determining the makespan of a set of jobs is a very challenging problem in scheduling theory. In the literature, extensive efforts have been made for the minimum makespan scheduling problem – that is, to find a priority assignment for all the jobs of \( J \) such that the makespan is minimized upon a given \( m \)-processor platform. Following the naming scheme introduced by Graham et al. [7], this problem is referred to as \( P||C_{\text{max}} \). However, in this paper, we will focus on the maximum makespan that could be produced by a given set of \( n \) jobs (all release at the same time), scheduled according to any work-conserving scheduler upon an \( m \)-processor uniform platform, in order to provide the time instants at which it is safe to enable the new-mode tasks after a MCR.

For a given set of jobs, an intuitive idea for maximizing the makespan upon an \( m \)-processor uniform platform would be to execute, at any time, the longest ready job upon the slowest available processor, i.e., the shorter the computation requirement of a job, the higher its priority. However, we can show that this intuitive idea is erroneous, unfortunately\(^4\). An FJP assignment leading to the maximum makespan remains an open question.

Another intuitive idea would be to naively extend one of the results proposed in [9] for an \( m \)-processor identical platform, i.e.,

\(^4\)On the 2-processor identical platform \( \pi = [1, 1] \), the set of jobs \( J = \{J_1, J_2, J_3, J_4\} \), all released at time \( t = 0 \) and such that \( C_1 = 2, C_2 = 3, C_3 = 5 \) and \( C_4 = 7 \) provides a makespan of 10 when \( J_1 > J_2 > J_3 > J_4, \) whereas the priority assignment \( J_3 > J_1 > J_2 > J_4 \) leads to a makespan of 12.

Lemma 5 (Lemma 5 in [9]) Let \( J = \{J_1, J_2, \ldots, J_n\} \) be a set of \( n \) jobs, all released at time \( t = 0 \), with computation requirements \( C_1, C_2, \ldots, C_n \), respectively, such that \( C_1 \leq C_2 \leq \cdots \leq C_n \). Suppose that these jobs are scheduled upon \( m \) identical processors by a work-conserving scheduler \( S \). Then, whatever the priority assignment of jobs, an upper bound on the makespan is given by

\[
\text{upms}(J, m) = \begin{cases} 
C_n & \text{if } m \geq n \\
\frac{1}{m} \sum_{i=1}^{n} C_i + \left(1 - \frac{1}{m}\right) C_n & \text{otherwise}
\end{cases}
\]

(2)

Naively extending Expression 2 leads to

\[
\text{upms}(J, m) = \begin{cases} 
C_n & \text{if } m \geq n \\
\frac{1}{m} \sum_{i=1}^{n} C_i + \left(1 - \frac{1}{m}\right) C_n & \text{otherwise}
\end{cases}
\]

(3)

and we can show that the intuitive idea used to derive this bound does not extend to uniform platforms, unfortunately\(^5\).

Now we are aware that neither the “Shortest-Job-First” policy nor upms\((J, \pi)\) lead to the maximum makespan. In Section 4, we present the protocols SUM-MSO and AUM-MSO that are generalizations to uniform multiprocessor platforms of the protocols SM-MSO and AM-MSO respectively, defined for identical multiprocessor platforms [9]. Then, we provide in Sections 6.1 and 6.2 two distinct upper bounds on the maximum makespan, for the cases where jobs priorities are known and unknown beforehand, i.e., FTP and FJP schedulers, respectively.

4. Protocols SUM-MSO and AUM-MSO

SUM-MSO. The protocol SUM-MSO which stands for “Synchronous Uniform Multiprocessor Minimum Single Offset” is an extension to uniform multiprocessor platforms of the protocol SM-MSO defined for identical multiprocessor platforms [9] to manage the rem-jobs during transition between any two operating modes. The main idea of SUM-MSO is the following: upon a MCR\( (j) \), every task of the current mode (say \( M' \)) is disabled and the rem-jobs continue to be scheduled by \( S \) upon the \( m \) processors. When all of them are completed, all the new mode tasks (i.e., the tasks of \( t' \)) are simultaneously enabled. We refer the interested reader to [9] for a pseudo-code of this protocol.

AUM-MSO. The protocol AUM-MSO which stands for “Asynchronous Uniform Multiprocessor Minimum Single Offset” is an extension to uniform multiprocessor platforms of the protocol AM-MSO defined for identical multiprocessor platforms [9] to manage the rem-jobs during transition between any two operating modes. The main
idea is the following: upon a MCR(\(j\)), reduce the mode-change delay applied to new-mode tasks by enabling them as soon as possible. Here, rem-jobs and new-mode tasks can be scheduled simultaneously during the transition phases according to the scheduler \(S^\text{trans}\) with the following rules: (i) the priorities of the rem-jobs are assigned according to the old-mode scheduler; (ii) the priorities of the new-mode tasks are assigned according to the new-mode scheduler, and (iii) every rem-job always has a higher priority than every new-mode task.

Upon a MCR(\(j\)), all the old-mode tasks, say of mode \(M^j\), are disabled and the rem-jobs continue to be scheduled by \(S^j\). Whenever the lowest priority rem-job migrates to a faster processor due to the completion of a higher priority one, (say at time \(t\)), some processors become available and thus the protocol AUM-MSO immediately enables some new-mode tasks; contrary to the protocol SUM-MSO which waits for the completion of all the rem-jobs. In order to select the new-mode tasks to enable at time \(t\), AUM-MSO uses the following heuristic: it considers every disabled new-mode task in increasing order of their mode-change deadlines and it enables those which can be scheduled by \(S^j\) upon the current available CPUs (i.e., the CPUs which are not running a rem-job and which are therefore available for executing some new-mode tasks).

Let \(\pi = [s_1, s_2, \ldots, s_m]\) be an \(m\)-processor uniform platform with processor capacities such that \(s_j \leq s_{j+1}\) for all \(j, 1 \leq j \leq m - 1\). Let \(S\) be any work-conserving FJP scheduler. Let \(\tau^i\) be a set of tasks. We denote by \(\pi_\ell(\tau^i)\) the subset of processors running a job of \(\tau^i\) when \(\tau^i\) is scheduled by \(S\) upon platform \(\pi\). We denote by CPU\((\pi, S, \tau^i)\) the binary function defined by:

\[
\text{CPU}(\pi, S, \tau^i) = \begin{cases} 
1 & \text{if } \pi_\ell(\tau^i) \text{ is schedulable by } S \text{ upon } \pi \\
0 & \text{otherwise}
\end{cases}
\]

This function is useful as we must always guarantee that all the deadlines are met for all the jobs in the system. To the best of our knowledge, there is no efficient necessary and sufficient schedulability test for most multiprocessor schedulers upon uniform platforms. However sufficient schedulability tests exist for scheduler such as EDF and DM [2, 3]. Algorithm 1 gives the pseudo-code of the AUM-MSO protocol in a more formal way.

### 5. Validity tests for protocols SUM-MSO and AUM-MSO

In the previous section we have defined the transition protocols SUM-MSO and AUM-MSO. Now, we need to establish a validity test – that is, a condition based on the tasks and platforms characteristics that indicates a priori whether the given system will always comply its expected requirement during every mode change. To do so, we proved in Lemma 3 that disabling the old-mode tasks upon a MCR does not jeopardize the schedulability analysis of the rem-jobs, when they continue to be scheduled by using the old-mode scheduler specifications upon the \(m\) processors. In Lemma 4 we defined the worst-case scenario.

#### 5.1. Validity test for SUM-MSO

Thanks to Lemma 3, the deadline of every rem-job is always met while using SUM-MSO during the transition phases. Thereby, SUM-MSO is valid for a given multi-mode real-time system if, for every mode change, the maximal transition delay which could be produced by the rem-jobs is not larger than the minimal mode-change deadline of the new-mode tasks. Thanks to Lemma 4, the transition delay which is actually equal to the completion time of all the rem-jobs is maximal when they are released simultaneously, with execution requirements equal to their WCETs. This leads to the following validity test.

**Validity Test 1** For any multi-mode real-time system \(\tau\) and any uniform platform \(\pi\), protocol SUM-MSO is valid provided \(\forall i, j\) with \(i \neq j\):

\[
\text{upms}(\tau^i, \pi) \leq \min_{1 \leq k \leq n_j} \{D_k(M^j)\}
\]

where upms\((\tau^i, \pi)\) is an upper-bound on the makespan and is defined in Sections 6.1 and 6.2 for both FTP and FJP schedulers, respectively.

#### 5.2. Validity test for AUM-MSO

The main idea to know whether AUM-MSO is valid for a given system \(\tau\) and platform \(\pi\) is to simulate Algorithm 1 for every possible mode transition, while considering the worst-case scenario for each one – the scenario where the new-mode tasks are enabled as late as possible. From our definition of protocol AUM-MSO, we know that every instant at which some new-mode tasks are enabled corresponds to an instant at which a processor has no more rem-job to execute, i.e., the “step instants” step\(_i\) of the
staircase depicted in Figure 1. Consequently, the largest instants at which new-mode tasks could be enabled are the upper-bounds \( \text{step}_j \), \( j = 1, 2, \ldots, m \) for both FTP and FJP schedulers. These upper-bounds are defined for both FTP and FJP schedulers in Sections 6.1 and 6.2, respectively. Notice that it results from this notation that \( \text{step}_m = \text{upms}(\tau', \pi) \) and the validity test for SUM-MSO can be rewritten as \( \text{upms}(\tau', \pi) \).

The details for the validity of the transition protocol AUM-SMO are provided by Algorithm 2. The correctness of our validity algorithm derives directly from the fact that every instant at which a new-mode task is enabled in Algorithm 2 is as large as possible. Notice that, since our validity test considers only the worst-case scenario for every mode transition, it could be some time-instants (in any mode transition) during the actual execution of the system at which the set of already enabled tasks benefits from a larger number of available processors than in the worst-case scenario. However, we prove in Lemma 6 that it does not jeopardize the system schedulability.

Lemma 6 Any predictable and work-conserving scheduler that is able to schedule a task set \( \tau \) upon a uniform platform \( \pi = \{s_1, \ldots, s_m\} \) is also able to schedule \( \tau \) upon any platform \( \pi^* \) such that \( \pi \subseteq \pi^* \).

Proof The proof is made by contradiction. To do so, it is sufficient to show the Lemma for \( \pi^* = \{s_1, \ldots, s_m, s_s\} \) where \( s_s \geq s_m \). Suppose there exists a task set \( \tau \) that is schedulable with a predictable and work-conserving scheduler \( S \) upon \( \pi \), but not upon \( \pi^* \supseteq \pi \). Consider the schedule of a particular instance \( I \) of \( \tau \) upon \( \pi^* \) leading to a deadline miss, and let \( I' \) be another instance of \( \tau \) derived from \( I \) reducing each job requirement by the amount of time each job executes upon the sub-platform \( \pi^* \setminus \pi \), i.e., upon \( \pi_s \). Since the scheduler is work-conserving, the schedule of \( I \) by \( S \) upon the processors in common with \( \pi \) is the same as the one that would be produced by \( S \) for \( I^* \) upon platform \( \pi^* \). Since a deadline is missed in the schedule of \( I \) upon \( \pi^* \), then a deadline is also missed in the schedule of \( I^* \) upon \( \pi \). But since the scheduler is predictable, a deadline would be missed on \( \pi \) even with the more demanding instance \( I \), leading to a contradiction. The lemma follows.

In the next sections, we determine the upper-bounds \( \text{step}_j \), \( j = 1, 2, \ldots, m \) for both FTP and FJP schedulers.

6. Determination of the upper-bounds \( \text{step}_j \)

6.1. Upper-bounds for FTP schedulers

We recall that for FTP schedulers job priorities are known beforehand.

Definition 6 \( \tau_j \) The time-instance \( \tau_j \) denotes the earliest instant in the schedule of the i highest priority jobs \( J_1, \ldots, J_i \), where at least \( i \) processors are idle (the processors \( \pi_1, \ldots, \pi_i \), since we consider work-conserving schedulers).

In Theorem 1 we provide the exact values of \( \tau_j \) \( \forall i \in \{1, 2, \ldots, n\} \) and \( \forall \pi \in \{1, 2, \ldots, m\} \) when each job executes for its WCET. As such we provide the exact value of \( \text{upms}_m \) which corresponds to the exact makespan for the scheduling of \( J = \{J_1, \ldots, J_n\} \) upon the platform \( \pi = \{s_1, \ldots, s_m\} \).

Theorem 1 Let \( J = \{J_1, J_2, \ldots, J_n\} \) be a set of \( n \) jobs, all released at time \( t = 0 \), with computation requirements \( C_1, C_2, \ldots, C_n \), respectively. Suppose that these jobs are scheduled according to a work-conserving FTP scheduler. Job \( J \) is ordered in decreasing-priority order then \( \tau_j \) is inductively defined as follows: (initialization) \( \tau_0 = 0 \), \( \forall j \leq m \) and \( \tau_{m+1} = \infty \), \( \forall i \), (iteration) \( \tau_{j+1} = \tau_j + \frac{C_j - \sum_{l=1}^{j} (t_{j+1} - t_{l-1}) \cdot s_l}{s_j} \) otherwise

Proof Initially, the \( m \) processors are idle, consequently \( \tau_0 = 0 \), \( \forall j \leq m \). We find convenient to define \( \tau_{m+1} = \infty \), \( \forall i \), which means that we have at most \( m \) processors available.

Now we will prove the correctness of the value of \( \tau_j \) \( \forall j \leq m \) assuming that \( \tau_{j-1} \) are defined \( \forall j \leq m + 1 \). The time-instants \( \tau_{j-1} \) define a staircase as illustrated in Figure 2 for the scheduling of jobs \( J_1, \ldots, J_{m-1} \). As such, job \( J_i \) can only progress during the grey areas. Consequently we have to distinguish between two cases:

1. \( \tau_{j-1} = \tau_{j+1} = t_j - t_{j-1} \), i.e., at least one faster processor becomes available at time \( t_j \) (the grey area on processor \( \pi_j \) is void in that case), the job \( J_i \) will be executed (if not completed) upon a faster processor, consequently the
first time-instant where at least \(j\) processors are idle remains unchanged and \(t'_{j} = t_{j}^{i-1}\).

2. Otherwise, \(J_i\) will be scheduled upon processor \(\pi_j\) while no faster processors become available or \(J_i\) completes. Remark that \(\sum_{j=1}^{n}(t'_{j+1} - t'_{j}) \cdot s_j\) corresponds to the grey area on processors \(\pi_1, \ldots, \pi_j\). Hence the two subsequent sub-cases follow.

**Figure 2. Staircase defined by the \(t_{j}^{i-1}\)**

**Corollary 1** Each instant \(t_{j}^{i} (\forall j = 1, 2, \ldots, m)\) defined in Definition 6 is an upper-bound on the “step-instant” \(t_{j}^{i}\) defined in Lemma 1, i.e., \(t_{j}^{i} \leq t_{j}^{i} (\forall j = 1, 2, \ldots, m)\). Therefore, the instants \(t_{j}^{i}\) (\(\forall j = 1, 2, \ldots, m\)) computed in Theorem 1 can be used as the instants \(t_{j}^{i}\) in the validity test provided by Algorithm 2.

**Proof** From Theorem 1, the instants \(t_{j}^{i}\) (\(\forall j = 1, 2, \ldots, m\)) are derived from the schedule in which every job executes for its WCET (we denote this “worst-case” schedule \(S_{wc}\) hereafter). Now, suppose by contradiction that in the actual schedule \(S_{act}\) (during the system execution), there exist \(j \in [1,m]\) such that \(t_{j}^{i}\) in \(S_{act}\) is strictly larger than \(t_{j}^{i}\) from \(S_{wc}\). This implies that, within the time interval \([t_{j}^{i}, t_{j}^{i}]\), there are at least \((m - j + 1)\) running jobs in \(S_{act}\) while there are at most \((m - j)\) running jobs in \(S_{wc}\). Therefore, within \([t_{j}^{i}, t_{j}^{i}]\), at least one job (say \(J_i\)) is not completed yet in \(S_{act}\) whereas it is already completed in \(S_{wc}\). But since we consider only work-conserving schedulers and since in \(S_{act}\) the execution requirement of \(J_i\) can only be lower than or equal to that in \(S_{wc}\), the fact that \(J_i\) completes later in \(S_{act}\) than in \(S_{wc}\) leads to a contradiction with the predictability.

### 6.2. Upper-bounds for FJP schedulers

We recall that for FJP schedulers job priorities are unknown beforehand. We assume without any loss of generality that we always have \(m \leq n\) as the problem in the case where \(m \geq n\) reduces to the same problem upon the \(n\) fastest processors. In Lemma 7, we first determine a lower bound on the smallest instant in the schedule of \(J\) where at least \(j\) CPUs (with \(j = 1, 2, \ldots, m\)) are idle. Then in Theorem 2 we determine an upper bound on the maximum makespan that could be produced by \(J\), this is given by \(\tau_{m}\).

**Lemma 7** Let \(J = \{J_1, J_2, \ldots, J_n\}\) be a set of \(n\) jobs with computation requirements \(C_1, \ldots, C_n\), respectively, such that \(C_1 \leq \cdots \leq C_n\). A lower bound \(\hat{L}_J\) on the smallest instant \(s_{j}\) at which at least \(j\) CPUs (with \(j = 1, 2, \ldots, m\)) are idle is given by

\[
\hat{L}_J = \frac{1}{S_{\pi}} \cdot \sum_{k=1}^{n-m+j} C_k \text{ where } S_{\pi} = \sum_{i=1}^{m} s_i \tag{4}
\]

**Proof** For the schedule \(S\) obtained from a work-conserving FJP scheduler, let \(s_{j}\), denote the smallest instant in \(S\) at which at least \(j\) processors are idle. According to Definition 1, at most \((m - j)\) jobs are not completed at time \(s_{j}\), meaning that at least \((n - m + j)\) jobs are already completed. If \(J'\) denotes any subset of \(r \geq (n - m + j)\) jobs of \(J\), then a lower bound \(t\) on the instant at which the \(r\) jobs of \(J'\) are completed is given by \(t \geq 1 \cdot \sum_{k \in J'} C_k\).

Obviously, since \(C_1 \leq C_2 \leq \cdots \leq C_n\), \(t\) is minimal for \(J' = \{J_1, J_2, \ldots, J_{n-m+j}\}\), i.e., \(t = \hat{L}_J\). The lemma follows.

**Theorem 2** Let \(J = \{J_1, J_2, \ldots, J_n\}\) be a set of \(n\) jobs with computation requirements \(C_1, \ldots, C_n\), respectively, such that \(C_1 \leq \cdots \leq C_n\). An upper bound \(\overline{s}_{j}\) on the smallest instant at which at least \(j\) CPUs (with \(j = 1, 2, \ldots, m\)) are idle is given by

\[
\overline{s}_{j} = \frac{\sum_{k=1}^{n} C_k - \sum_{k=j+1}^{n} \hat{L}_k \cdot s_k}{\sum_{k=j}^{m} s_k} \tag{5}
\]

**Proof** Consider the following notations: (i) \(S\) denotes the schedule of the \(n\) jobs obtained from a work-conserving FJP scheduler; (ii) \(s_{j}\), (with \(j = 1, 2, \ldots, m\)) denotes the smallest instant in \(S\) at which at least \(j\) processors are idle, and (iii) \(W_j\) denotes the amount of work executed on CPU \(\pi_j\) within \([0, t_{j}]\), i.e., \(W_j \equiv s_{j}\). Let \(k\) be any integer in \([1, m]\) and suppose by contradiction that \(s_{k} > s_{k}\) cannot be true.

By definition of the \(W_j\), we know that

\[
\sum_{j=1}^{m} W_j = \sum_{j=1}^{n} C_j \tag{6}
\]

Furthermore, we know that \(\sum_{j=1}^{m} W_j = \sum_{j=1}^{k} W_j \cdot s_{j} = \sum_{j=1}^{k} (s_{j} \cdot s_{j}) + \sum_{j=k}^{m} (s_{j} \cdot s_{j})\). Since we know from Lemma 1 that we have \(s_{j} \geq s_{j}\) for all \(j = 1, 2, \ldots, m - 1\), it holds that

\[
\sum_{j=1}^{m} W_j \geq \sum_{j=1}^{k} (s_{j} \cdot s_{j}) + \sum_{j=k}^{m} (s_{j} \cdot s_{j})
\]
By assumption we have \( \text{step}_k > \text{step}_{k+1} \), leading to
\[
\sum_{j=1}^{m} W_j > \sum_{j=1}^{k-1} (\text{step}_j \cdot s_j) + \text{step}_k \cdot \sum_{j=k}^{m} s_j
\]
\[
> \sum_{j=1}^{k-1} (\text{step}_j \cdot s_j) + \frac{\sum_{j=1}^{m} C_j - \sum_{j=k}^{m} \hat{L}_j \cdot s_j}{\sum_{j=k}^{m} s_j} \sum_{j=k}^{m} s_j
\]
\[
> \sum_{j=1}^{n} C_j + \sum_{j=1}^{k-1} \left( (\text{step}_j - \hat{L}_j) \cdot s_j \right)
\]

Since from Lemma 7 it holds that \( \hat{L}_j \leq \text{step}_j \) \( \forall j = 1, 2, \ldots, m \), it yields \( \sum_{j=1}^{m} W_j > \sum_{j=1}^{m} C_j \) leading to a contradiction with Equality 6. The theorem follows. \( \blacksquare \)

### 7. Experimental results

For experimental purpose, let us recall the definition of the parameter \( \lambda_{\pi} \) [6] for an \( m \)-processor uniform platform \( \pi = [s_1, s_2, \ldots, s_m] \): 
\[
\lambda_{\pi} \text{ def } = \max_{j=1}^{m} \left\{ \sum_{i=1}^{j-1} s_i \right\} \]
Note that parameter \( \lambda_{\pi} \) measures the “degree” by which \( \pi \) differs from an identical multiprocessor platform.

In this section, we report on the results of experiments conducted using the theoretical results presented in Section 6.2 (since the upper-bounds presented in Section 6.1 can be considered as exact if every job executes for its WCET). The considered set of jobs \( J \) is composed of 10 jobs of undetermined priority and the platform \( \pi \) is composed of 4 processors with computing capacities varying within \([1, 101]\) with an increment of 10.

During the simulation, all possible combinations of the processors speeds are considered for the 4 CPUs. For every assignation of processors speed, we determine the corresponding parameter \( \lambda_{\pi} \) as well as the error \( E(J, \pi) \) (expressed in percent) of upms \( J, \pi \) compared to the exact value of the maximum makespan (which is determined by considering the schedules derived from every job priority assignment). Finally, the errors \( E(J, \pi) \) are displayed relative to the corresponding \( \lambda_{\pi} \) in Figure 3.

![Figure 3. Simulation results](image)

The most important error that we obtained is 10.64% and the minimal one is 2.28%. The average error is 7.78% with a squared distance of 2.32%. Hence, we believe that this is a promising path to go for more competitive bounds and for practical use.

### 8. Conclusion and Future work

In this paper, the scheduling problem of multi-mode real-time systems upon uniform multiprocessor platforms is studied. Two protocols for transitioning between every pair of operating modes of the system are specified together with their validity tests. The first proposed protocol SUM-MSO is synchronous in the sense that the tasks of the old- and new-mode are not scheduled simultaneously. The second protocol AUM-MSO is asynchronous in the sense that it allows old- and new-mode tasks to be scheduled together. This study led us to provide the reader with tight bounds for the length of the transient phases during mode transitions. Future work will focus on handling mode-independent tasks, i.e., tasks whose behavior is not affected by the mode changes.

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### References